Assignment 4 (2023-01-05)

1. Design a four stage pipelined processor supporting MIPS add instructions in Verilog HDL. Please download proc01.v from the support page and refer it.
2. Verify the behavior of designed processor using following assembly code assuming initial values of r[1]=22, r[2]=33, r[3]=44, and r[4]=55
   - `add $0, $0, $0 # NOP {6'h0, 5'd0, 5'd0, 5'd0, 5'd0, 6'h20}`
   - `add $1, $1, $1 #`
   - `add $2, $2, $2 #`
   - `add $3, $3, $3 #`
   - `add $4, $4, $4 #`
3. Submit a report printed on A4 paper at the beginning of the next lecture on **Thursday**. Or,
   Submit your report in a PDF file via E-mail (kise [at] c.titech.ac.jp) by the beginning of the next lecture on **Thursday**.
   - The report should include a block diagram, a source code in Verilog HDL, and obtained waveforms of your design.
   - E-mail title should be "Assignment of Advanced Computer Architecture"