Assignment 3 (2022-12-22)

1. Design a single-cycle processor supporting MIPS add, addi, lw and sw instructions in Verilog HDL.
2. Verify the behavior of designed processor using following assembly code
   - `add  $0,  $0,  $0  # NOP {6'h0, 5'd0, 5'd0, 5'd0, 5'd0, 6'h20}`
   - `addi $8, $0, 8     # {6'h8, 5'd0, 5'd8, 16'd8}, $8 = 8`
   - `sw   $8, 4($8)     # {6'h2b,5'd8, 5'd8, 16'd4}, mem[12] = 8`
   - `lw   $9, 4($8)     # {6'h23,5'd8, 5'd9, 16'd4}, $9 = mem[12]`
   - `addi $10, $9, 6    # {6'h8, 5'd9, 5'd10,16'h6}, $10 = $9 + 6`
3. Submit your report in a PDF file via E-mail (kise [at] c.titech.ac.jp) by 13:00 on January 5th.
   - The report should include a block diagram, a source code in Verilog HDL, and obtained waveforms of your design.
   - E-mail title: Assignment of Advanced Computer Architecture