Assignment 2, sama as assignment 1 (2022-12-19)

1. Design a single-cycle processor supporting MIPS add, addi instructions in Verilog HDL. Please download proc01.v from the support page and refer to it.
2. Verify the behavior of designed processor using following assembly code
   - `add  $0, $0, $0   # {6'h0, 5'd0, 5'd0, 5'd0, 5'd0, 6'h20}`
   - `addi $7, $0, 3    # {6'h8, 5'd0, 5'd7, 16'd3}`
   - `addi $8, $0, 5    # {6'h8, 5'd0, 5'd8, 16'd5}`
   - `add  $9, $7, $8   # {6'h0, 5'd7, 5'd8, 5'd9, 5'd0, 6'h20}`
3. Submit a report printed on A4 paper at the beginning of the next lecture on Monday. Or,
   Submit your report in a PDF file via E-mail (kise [at] c.titech.ac.jp) by the beginning of the next lecture on Monday.
   - The report should include a block diagram, a source code in Verilog HDL, and obtained waveforms of your design.