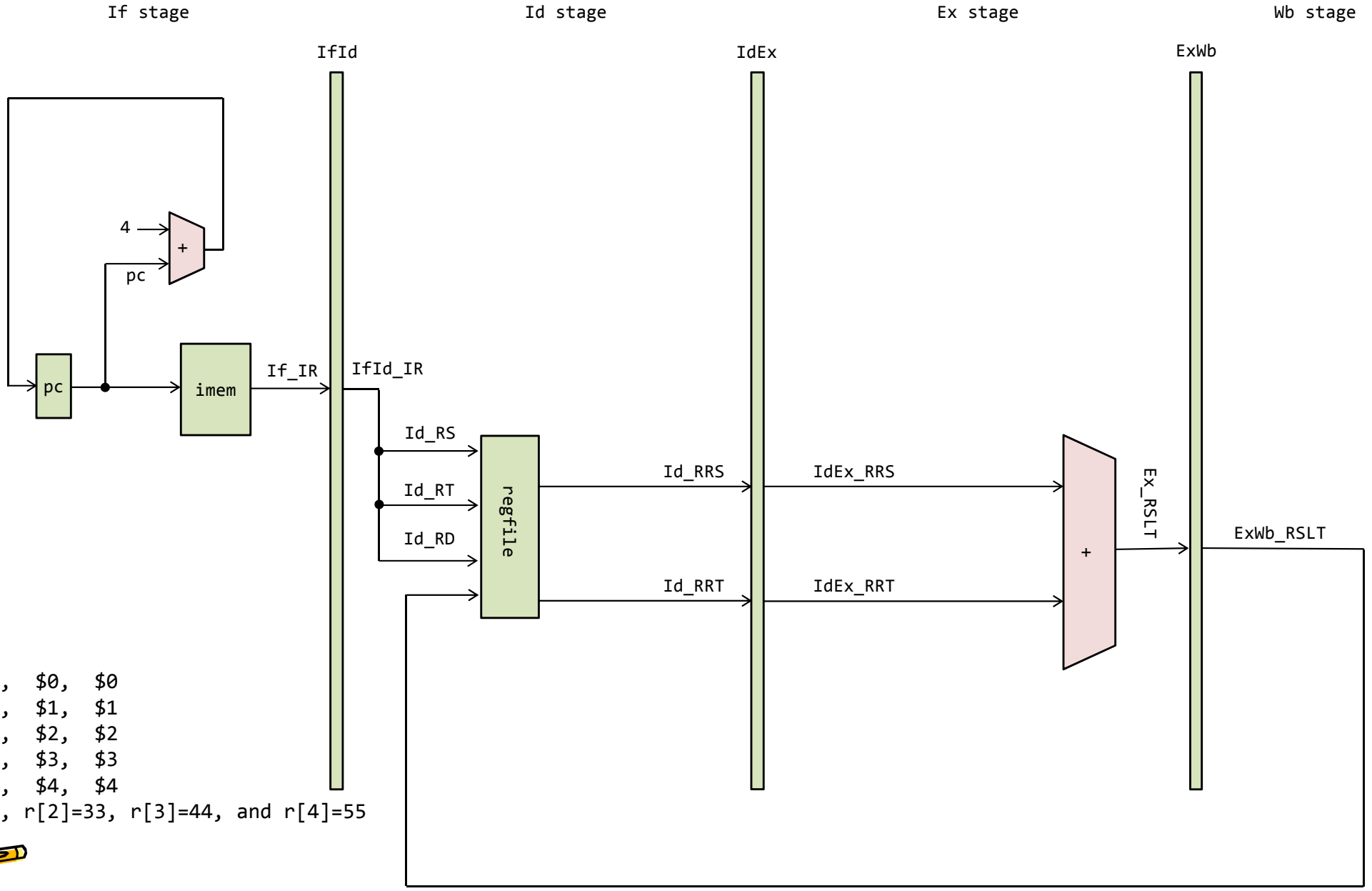
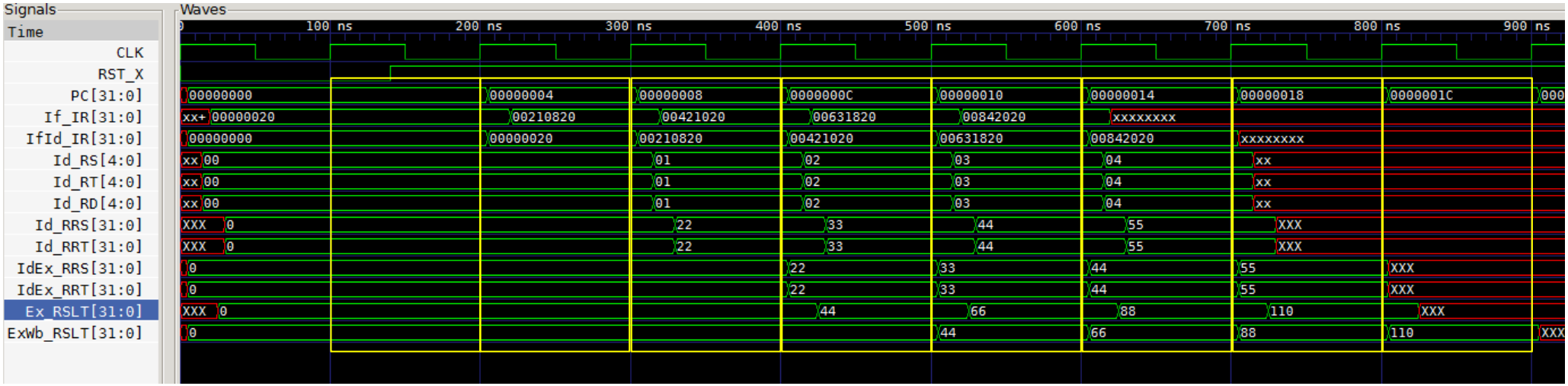
Four stage pipelined processor supporting ADD, which uses wrong RD and does not adopt data forwarding (proc05.v)




```
add  $0,  $0,  $0
add  $1,  $1,  $1
add  $2,  $2,  $2
add  $3,  $3,  $3
add  $4,  $4,  $4
r[1]=22, r[2]=33, r[3]=44, and r[4]=55
```

Waveform of Proc05

- Please confirm that the values in regfile are wrong




```
0x00 add  $0,  $0,  $0     IF        ID        EX        WB
0x04 add  $1,  $1,  $1               IF        ID        EX        WB
0x08 add  $2,  $2,  $2                         IF        ID        EX        WB
0x0C add  $3,  $3,  $3                                   IF        ID        EX        WB
0x10 add  $4,  $4,  $4                                             IF        ID        EX        WB
```

r[1]=22, r[2]=33, r[3]=44, and r[4]=55

Four stage pipelined processor supporting ADD, which does not adopt data forwarding (proc06.v, Homework 4)