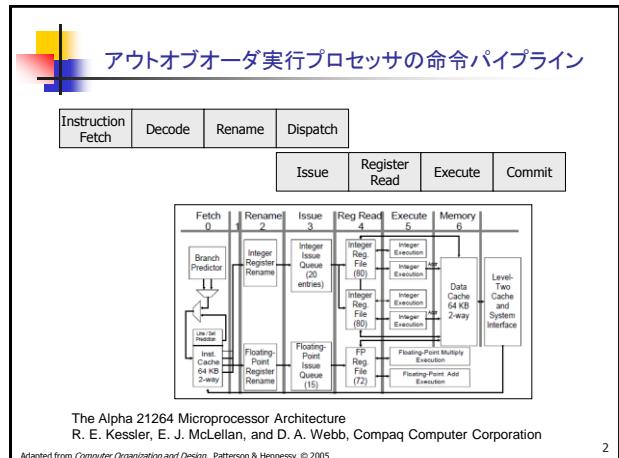


2011年 後学期

## 計算機アーキテクチャ 第二 (O)

### データ値予測, データフロー実行モデル

1



### 命令発行機構: Tomasuloのアプローチ

- IBM 360/91 の浮動小数点ユニットでは、アウトオブオーダ実行

The IBM 360/91

Installation of the IBM 360/91 in the Columbia Computer Center machine room in February or March 1969. Photo: AIS archive.

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### 命令発行機構: Tomasuloのアプローチ 1967

- IBM 360/91 の浮動小数点ユニットでは、アウトオブオーダ実行のための洗練された方式が採用されていた。
- Robert Tomasulo によって発明されたこの手法では
  - (1) レジスタリネーミングを導入してWAWハザードとWARハザード(偽のデータ依存)を排除
  - (2) 命令が必要とするオペランドがいつ利用できるかを探知し, RAW(Read after Write)ハザードを最小化
- 近年のプロセッサでは、この手法のさまざまなバリエーションが採用されているが、これら2つの重要な概念は共通の特徴

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### マルチレベル・ストライ値予測機構による命令レベル並列性の向上 (JSPP 1999)

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### 研究の背景

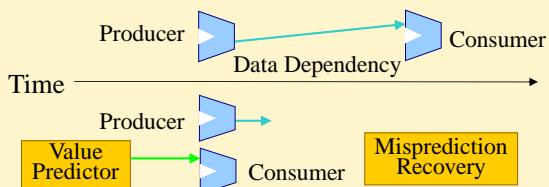
- 真のデータ依存関係が命令レベル並列性を制限
- 生産者から消費者へのデータの流れを解消する技術として値予測

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## 研究の背景

- 真のデータ依存関係が命令レベル並列性を制限
- 生産者から消費者へのデータの流れを解消する技術として値予測



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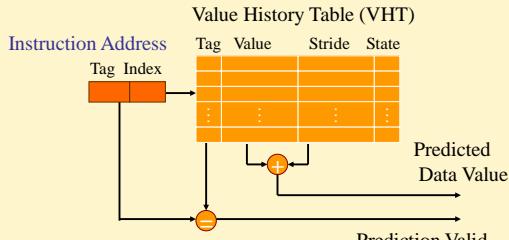
## 関連研究: 値生成のアルゴリズム

- Last-value予測
  - 最も近い過去に得られた値を予測値
- ストライド値予測
  - 最も近い過去に得られた2回の値の差分 Stride と、Last-value の和を予測値
- 2レベル値予測
  - 過去のn個の履歴の中からひとつを選択
- ハイブリッド値予測
  - 複数のアルゴリズムから選択

Adapted from Computer Organization and Design, Patterson & Hennessy, © 2005

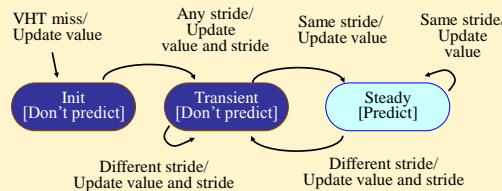
## ストライド値予測機構

$$\text{Predicted Value} = \text{Last-value} + \text{Stride}$$



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## ストライド値予測機構 (cont.)



Stateフィールドの推移と予測アルゴリズム

Adapted from Computer Organization and Design, Patterson & Hennessy, © 2005

## ストライド値予測機構 (cont.)

1~5の値を繰り返す下の例

Value :	1	2	3	4	5	1	2	3	4	5	..
Stride:	1	1	1	1	-4	1	1	1	1	1	..
Result:	NP	NP	NP	H	H	M	NP	NP	H	H	..
State :	I	T	S	S	S	T	T	S	S	S	..

NP=No Predict, H=Hit, M=Miss

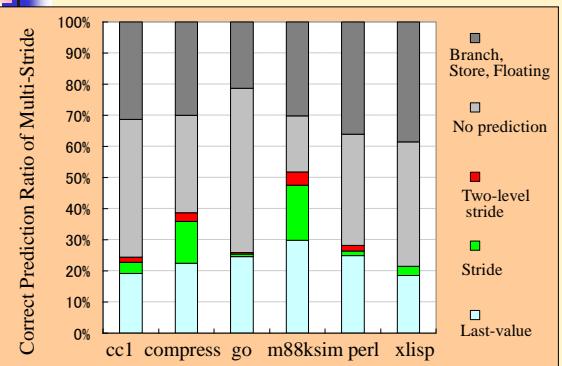
I=Initial, T=Transient, S=Steady

短い間隔でストライドが変化する場合に予測精度が低下、予測成功率40%

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## Multi-stride値予測の予測成功率



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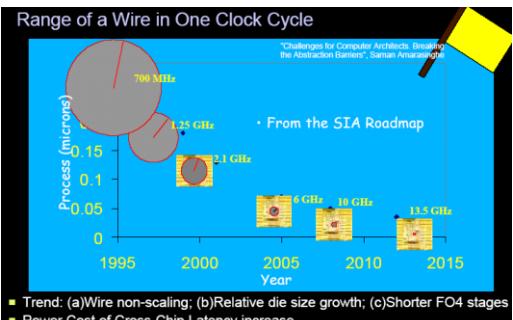
## 値予測ミスの回数とミス率

Program	Last-value	Stride	2-level Str.
<b>cc1</b>	10734(.05%)	33591(.77%)	13287(.68%)
<b>compress</b>	2679(.02%)	3094(.05%)	1489(.01%)
<b>go</b>	1934(.01%)	4827(.37%)	593(.11%)
<b>m88ksim</b>	16262(.04%)	43832(.20%)	29041(.53%)
<b>perl</b>	1245(.01%)	1544(.11%)	2950(.01%)
<b>xlisp</b>	1904(.02%)	2950(.24%)	9(.05%)

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## Range of a Wire in One Clock Cycle



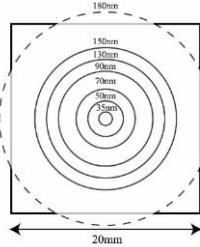
MICRO-36 (2003, San Diego, CA) Keynote Kerry Bernstein Senior Technical Staff Member IBM T.J. Watson Research Center

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## 配線遅延の克服

- クロックサイクルの間に信号が伝わるチップ内の範囲
  - 8 FO4 を1クロック
  - 20 x 20mm のチップ
- 35nm のテクノロジ
  - 1クロックで信号を伝達可能な範囲は全体の1%
  - 距離の離れた2点間では、数十サイクルの遅延
- 配線遅延を考慮して方式を検討

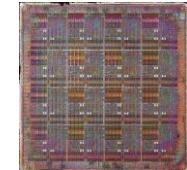
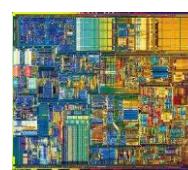


[1] S.W. Keckler, Doug Burger, C.R. Moore, R. Nagarajan, K. Sankaralingam, V. Agarwal, M.S. Hirshikesh, N. Ranganathan, and P. Shivakumar, A Wire-Delay Scalable Microprocessor Architecture for High Performance Systems, International Solid-State Circuits Conference (ISSCC), pp.1068-1069, February 2003.

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## タイルアーキテクチャとは

- 小さいサイズの機能ブロック(タイル)を規則的に敷きつめることで高速なプロセッサを構成する方式
  - タイルのサイズを小さくすることで、タイルの内部で発生する配線遅延の問題を軽減
  - 近くに配置されているタイル間でのみデータの送受信をおこなうことで、タイル間の通信遅延を軽減
  - 同じ構成のタイルを複製して、設計と検証の作業の簡略化



スーパースカラのPentium 4プロセッサと、タイルアーキテクチャのRawプロセッサ

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## タイル

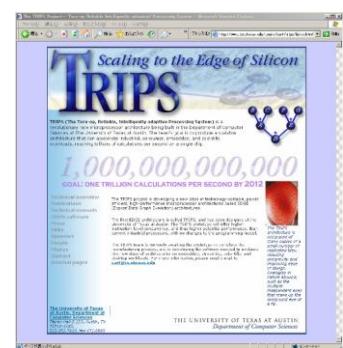
- 「壁または床などに張る小片状の薄板。陶磁器が一般的」  
広辞苑
- 「Tiles are flat, square pieces of baked clay, carpet, cork, or other substance, which are fixed as a covering onto a floor or wall.」 Collins COBUILD English Dictionary

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## TRIPSプロセッサ

- テキサス大学におけるタイルプロセッサ
  - 単純な構成の計算ノード
  - 独自の実行モデル
  - 挑戦的



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## Explicit Dataflow Graph Execution (EDGE)

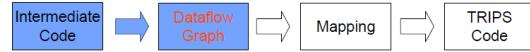
- Explicit Data Graph Execution
  - Defined by two key features

1. Program graph is broken into sequences of *blocks*
  - Basic blocks, hyperblocks, or something else
  - Blocks commit atomically or not at all - a block never partially executes
2. Within a block, ISA support for direct producer-to-consumer communication
  - No shared named registers within a block (point-to-point dataflow edges only)
  - The block's dataflow graph (DFG) is explicit in the architecture
  - Caveat: memory is still a shared namespace (bane of prior dataflow machines)

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## Block Compilation



### Intermediate Code

```

i1 add r1, r2, r3
i2 add r7, r2, r1
i3 ld r4, (r1)
i4 add r5, r4, #1
i5 beqz r5, 0xdeac
  
```

- Inputs (r2, r3)
- Temporaries (r1, r4, r5)
- Outputs (r7)



Compiler Transforms

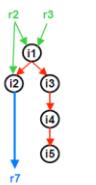
Lecture Note for CS352 Computer Systems Architecture by Prof. S.W. Keckler

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## Block Mapping



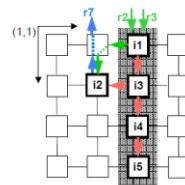
### Data flow graph



Scheduler

Scheduling is an optimization, not necessary for correctness

### Mapping onto array



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## TRIPS Block Example

### RISC code

```

ld R3, 4(R2)
add R4, R1, R3
st R4, 4(R2)
addi R5, R4, #2
beqz R4, Block3
  
```

- Read target format
- Predicated instructions
- LD/ST sequence numbers
- Target fanout with movs
- Block outputs fixed (3 in this example)

### TIL (operand format)

```

.bbegin block1
read $t1, $q1
read $t2, $q2
ld $t3, 4($t2)
add $t4, $t1, $t3
st $t4, 4($t2)
addi $t5, $t4, 2
teqz $t6, $t4
b_t<$t6> block3
b_f<$t6> block2
write $q5, $t5
.bend block1
.bbegin block2 ...
  
```

### TASL (target format)

[R1]	\$q1	[2]
[R2]	\$q2	[1]
[1]	ld	L:1 4 [2]
[2]	add	[3] [4]
[3]	mov	[5] [6]
[4]	st	S:2 4
[5]	addi	2 [W1]
[6]	teqz	[7] [8]
[7]	b_t	block3
[8]	b_f	block2
[W1]	\$q5	

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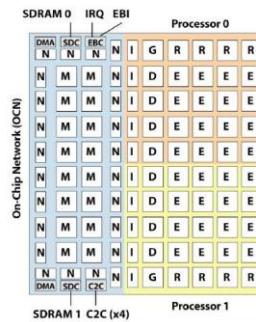
## TRIPS Block Format

PC →	Header Chunk	128 Bytes	Each block is formed from two to five 128-byte program "chunks"
	Instruction Chunk 0	128 Bytes	Blocks with fewer than five chunks are expanded to five chunks in the L1 I-cache
	Instruction Chunk 1	128 Bytes	Header chunk includes a block header: <ul style="list-style-type: none"> <li>□ Read/Write instructions</li> <li>□ Block header (8 bits)</li> <li>□ Block type (8 bits) - 1-4 instruction chunks</li> <li>□ Store mask (32 bits)</li> <li>□ Block occupancy flags (8 bits)</li> <li>□ Controls predictors on per-block basis</li> <li>□ Memory synchronization before/after block</li> <li>□ Breakpoint before/after block</li> </ul>
	Instruction Chunk 2	128 Bytes	Each instruction chunk holds 32 4-byte instructions (including NOPs)
	Instruction Chunk 3	128 Bytes	A maximally sized block contains 128 regular instructions, 32 read instructions, and 32 write instructions

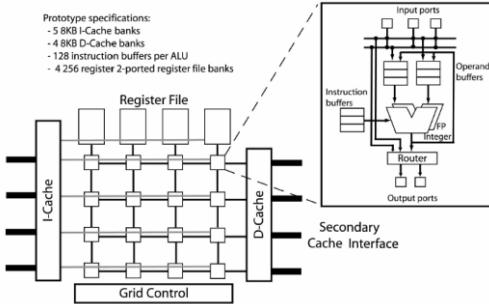
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## TRIPS Tile-level Microarchitecture



## 4×4の計算ノードを持つTRIPSプロセッサ、計算ノード構成

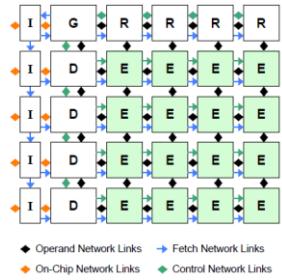


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## TRIPS Processor Tiles

- Partition all major structures into banks, distribute, and interconnect
- Execution Tile (E)
  - 64-entry Instruction Queue bank
  - Single-issue execute pipeline
- Register Tile (R)
  - 32-entry Register bank (per thread)
- Data Tile (D)
  - 8KB Data Cache bank
  - LSQ and MUH banks
- Instruction Tile (I)
  - 16KB Instruction Cache bank
- Global Control Tile (G)
  - Tracks up to 8 blocks of insts
  - Branch prediction & resolution logic

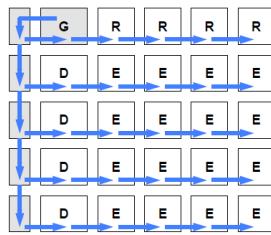


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## Block Fetch

- Fetch commands sent to each Instruction Cache bank
- The fetch pipeline is from 4 to 11 stages deep
- A new block fetch can be initiated every 8 cycles
- Instructions are fetched into Instruction Queue banks (chosen by the compiler)
- EDGE ISA allows instructions to be fetched out-of-order

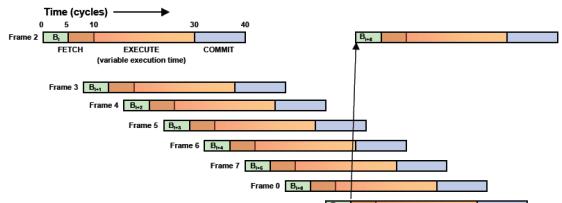


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## Block Execution Timeline



- Execute/commit overlapped across multiple blocks
- G-tile manages frames as a circular buffer
  - D-morph: 1 thread, 8 frames
  - T-morph: up to 4 threads, 2 frames each

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## Processor Performance

Name	TRIPS Speedup	Alpha IPC	TRIPS IPC	TRIPS Inst/Block	Description
a2time	5.05	0.81	4.05	77	Control, integer math
bezier	3.30	1.05	3.20	76	Bezier curve, fixed-point math
dct8x8	2.66	1.70	4.70	90	2D discrete cosine transform
matrix	3.30	1.68	4.05	72	Matrix multiply
sha	0.92	2.28	2.10	80	Secure hash (mostly sequential algorithm)
vadd	1.92	3.04	6.51	74	Vector add (limited by load/store bandwidth)

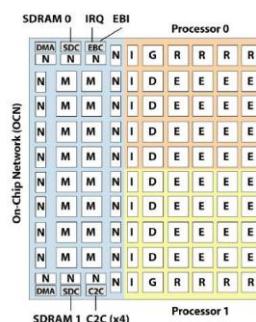
Simulated on TRIPS and Alpha 21264 cycle simulators  
Alpha compilation with GEM compiler and maximum opts (O4 and tuned for 21264)  
TRIPS compilation with in-development compiler plus some hand-tuning  
Speedup measured by comparing Alpha cycles to TRIPS cycles

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## TRIPS Tile-level Microarchitecture



- TRIPS Tiles**
- G: Processor control - TLB w/ variable size pages, dispatch, next block predict, commit
  - R: Register file - 32 registers x 4 threads, register forwarding
  - D: Data cache - 8KB per tile, 256-entry load/store queue, TLB
  - E: Execution unit - Int/FP ALUs, 64 reservation stations
  - M: Memory - 64KB, configurable as L2 cache or scratchpad
  - N: OCN network interface - router, translation tables
  - DMA: Direct memory access controller
  - SDC: DDR SDRAM controller
  - EBC: External bus controller - interface to external PowerPC
  - C2C: Chip-to-chip network controller - 4 links to XY neighbors

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2011年 後学期

## 計算機アーキテクチャ 第二 (O)

マルチコア、メニーコアへ

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### Growth in clock rate of microprocessors

From CAQA 5<sup>th</sup> edition 32

Adapted from *Computer Organization and Design*, Patterson & Hennessy, © 2005

### Growth in processor performance

From CAQA 5<sup>th</sup> edition 33

Adapted from *Computer Organization and Design*, Patterson & Hennessy, © 2005

### ムーアの法則によるトランジスタ数の増加

**ムーアの法則**  
チップで利用できるトランジスタの数は2年間で2倍に増加する。

プロセッサ	出荷年	トランジスタ数
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium III processor	1999	24,000,000
Pentium 4 processor	2000	42,000,000

ムーアの法則に従ってトランジスタ数が増加してきた。今後も同様の増加が見込まれる。  
出典：Intel社, <http://www.intel.com/research/silicon/mooreslaw.htm>

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### Tomasuloのアプローチ

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Adapted from *Computer Organization and Design*, Patterson & Hennessy, © 2005

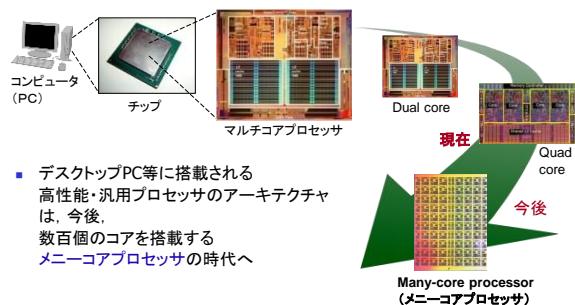
### ポラックの法則

- プロセッサの性能は、複雑性の平方根に比例する

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Adapted from *Computer Organization and Design*, Patterson & Hennessy, © 2005

## マルチコア(2個～数10個)からメニーコアへ



Adapted from *Computer Organization and Design*, Patterson & Hennessy, © 2005

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## アナウンス

- 講義スライド、講義スケジュール
  - [www.arch.cs.titech.ac.jp](http://www.arch.cs.titech.ac.jp)

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