A Super Instruction-Flow Architecture

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Abstract

Microprocessor performance has improved at about 55% per year over the past three decades. To maintain the performance growth rates, next generation processors with more than one billion transistors must achieve higher levels of parallelism. In this context, new paradigm or new architecture is required to attain a dramatic boost of available instruction level parallelism.

Most of the high performance processors in the market predict control-flow using a sophisticated branch predictor. However, even if a processor uses one of the latest branch predictors, such as YAGS[1], the prediction accuracy is about 95% at most. A branch predictor cannot avoid the misprediction of a fixed rate. In order to reduce the overhead of a branch instruction, in addition to the effort to reduce the number of mispredictions, the reduction of misprediction penalties becomes important.

The aim of this project is to develop a novel processor architecture which mitigates the performance degradation caused by the branch instructions. In order to solve the problem, we propose a super instruction-flow architecture. This architecture is a type of decoupled architecture[2]. It has the mechanism to processes the multiple instruction flows efficiently. In addition to the architectural proposal, we described the design of its first generation processor.

We report the preliminary evaluation results of the first generation super instruction-flow processor. Evaluation result show that the super instruction-flow processor with 5-stage pipeline achieves about 26% speedup compared with the conventional scalar processor. And the processor with 10-stage pipeline achieves the 33% speedup for matrix multiplication and the 29% speedup for selection sort. These evaluation results indicates that the super instruction-flow architecture effectively mitigates the overhead caused by a branch misprediction.

References

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